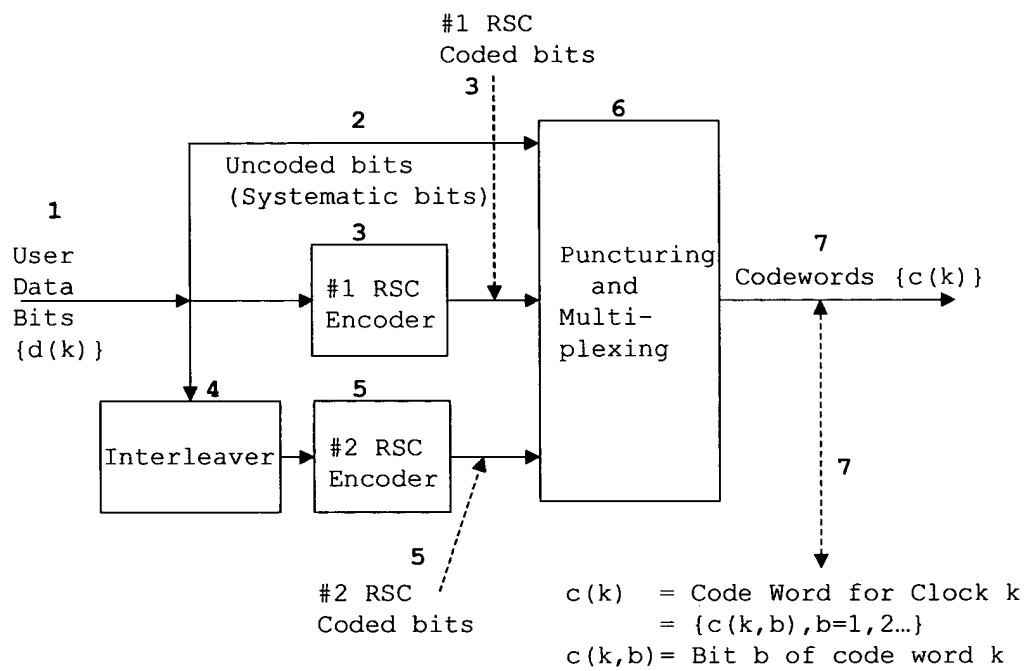


DRAWINGS

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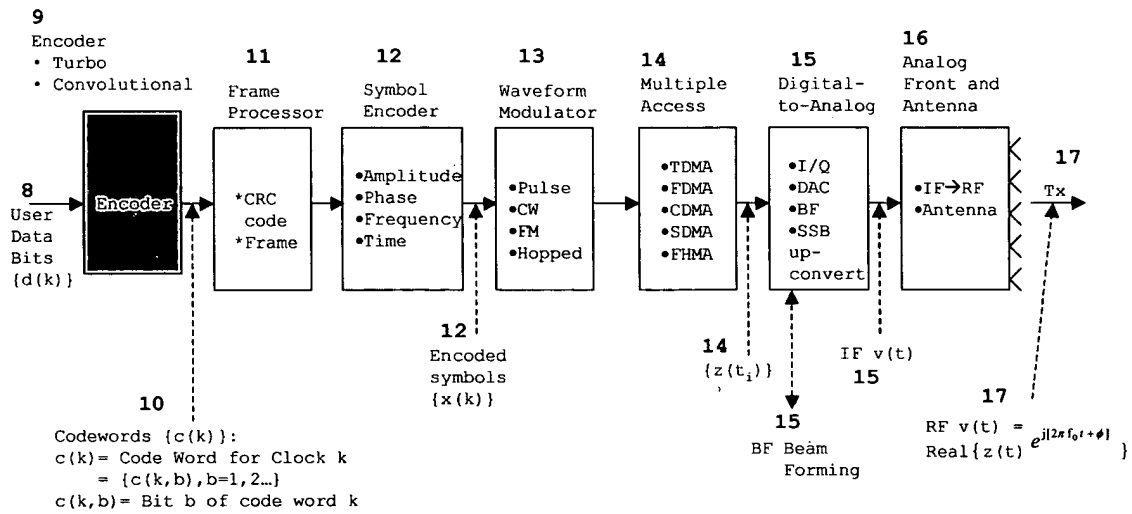
FIG. 1 Turbo Encoder Block Diagram for Parallel Architecture



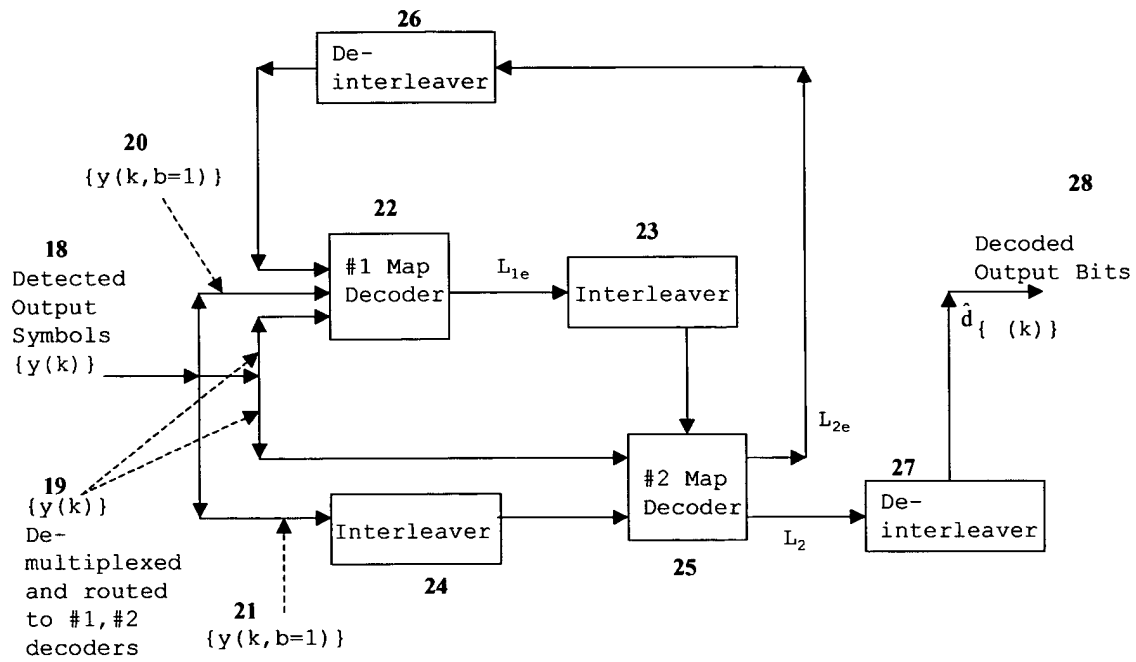
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FIG. 2 Turbo/Convolutional Code Transmitter Block Diagram



**FIG. 3 Iterative Turbo Decode Block Diagram
for Parallel Architecture**



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**FIG. 4 Turbo/Convolutional Code Receiver
Block Diagram**

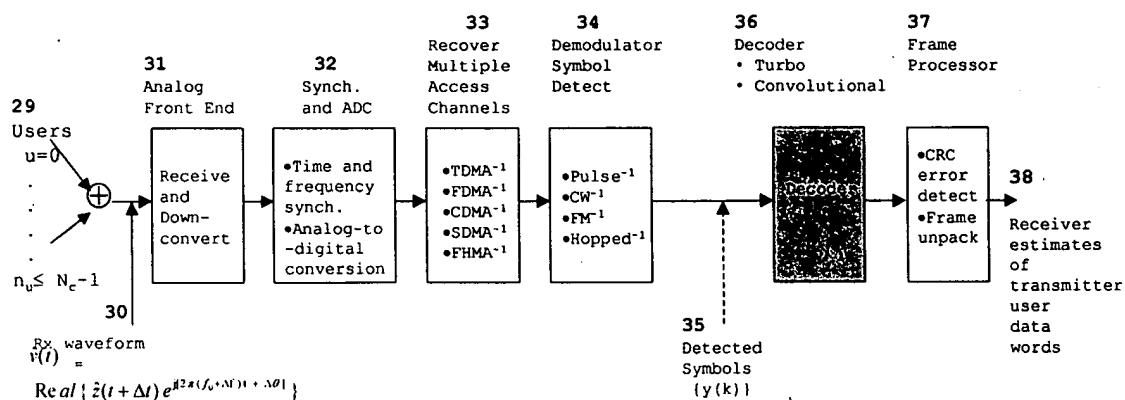
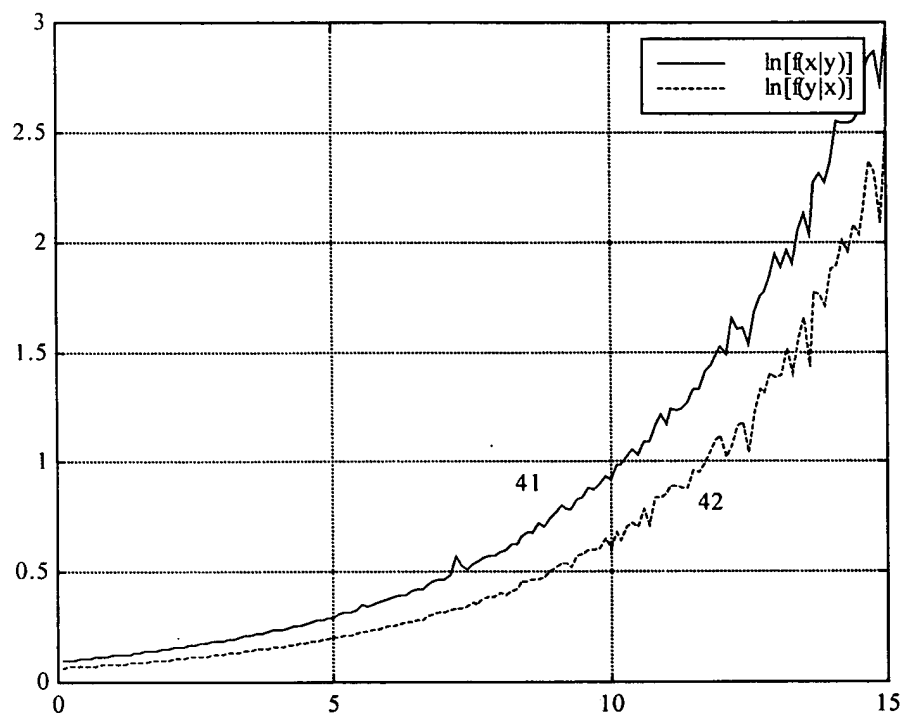


FIG. 5 Performance our MX decisioning metric $\ln[f(x|y)]$ vs. the ML decisioning metric $\ln[f(y|x)]$



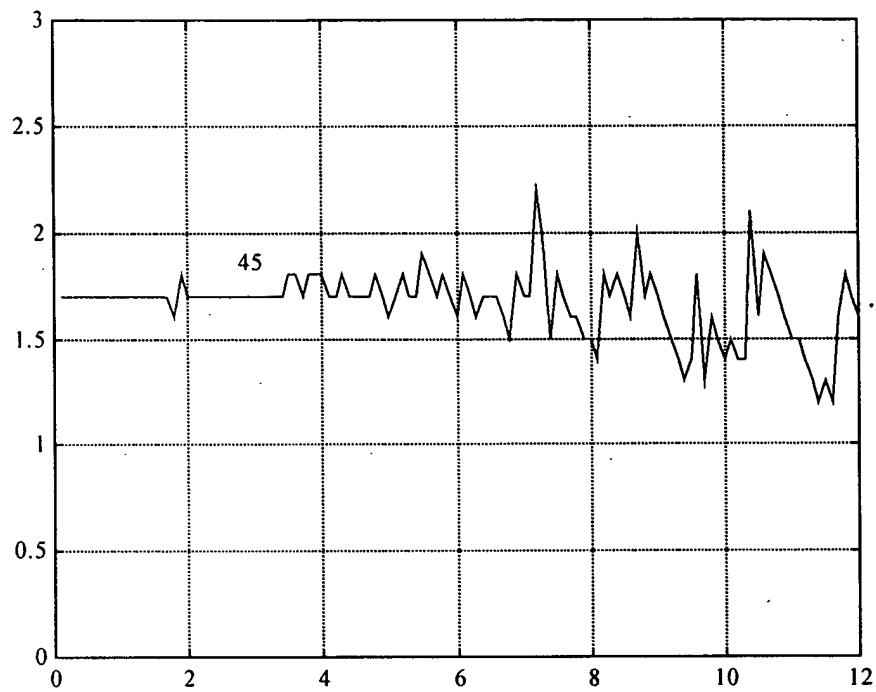
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**FIG. 6 Improvement in S/N using our new MX
Decisioning metric DX vs. the ML metric DM**



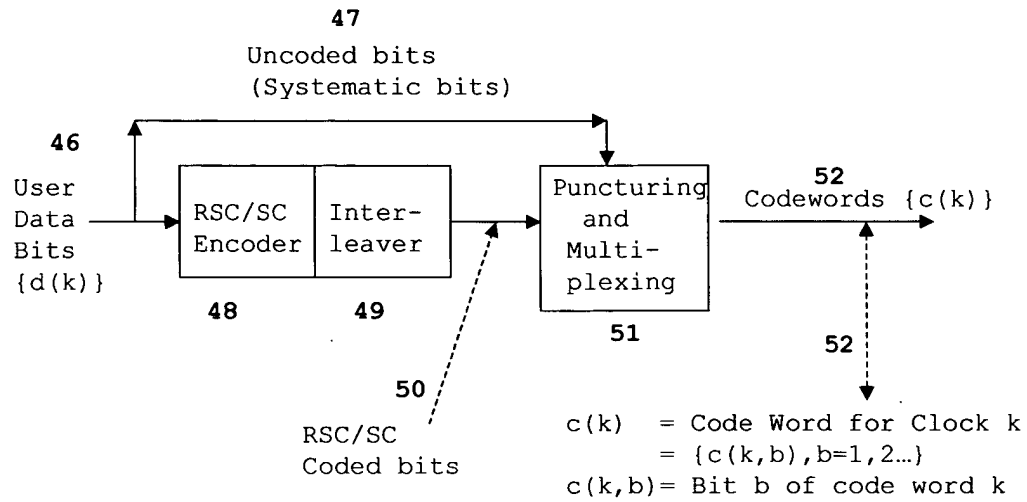
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FIG. 7 Convolutional Encoder Block Diagram



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FIG. 7 Convolutional Encoder Block Diagram

